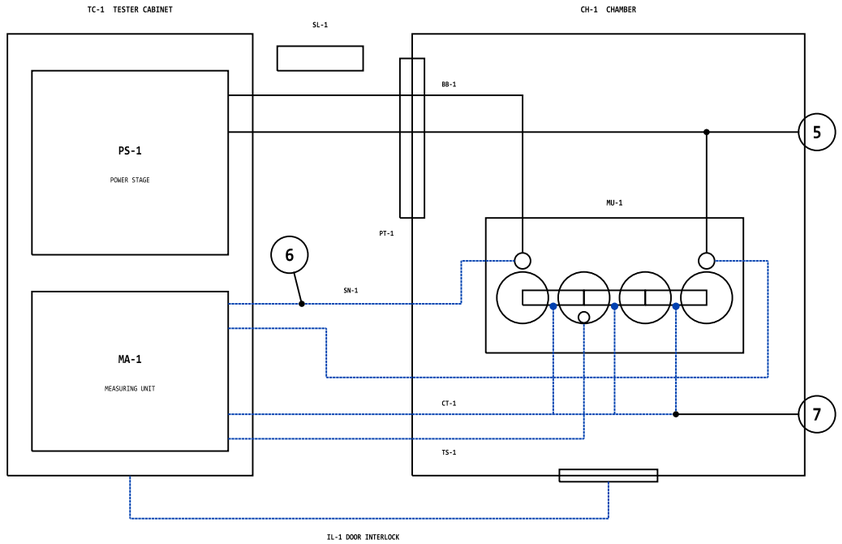
PLAN - TEST SYSTEM

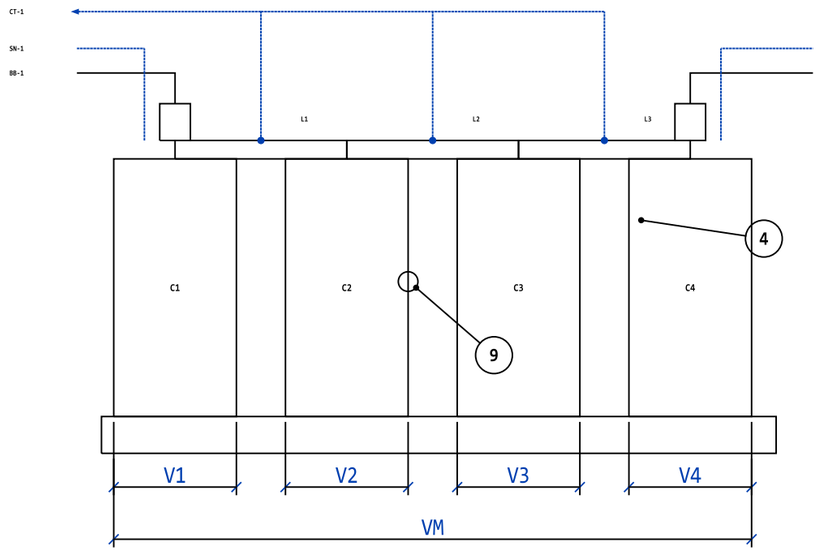
NOT TO SCALE



THE VOLTAGE VM ACROSS THE MODULE IS THE SUM OF THE CELL VOLTAGES V1 TO V4; A TAP ON EVERY LINK SHOWS HOW IT IS SHARED, AND THE SENSE WIRES TOUCH THE TERMINALS, NOT THE BUSBARS; C1 TO C4 ARE THE CELLS, L1 TO L3 THE LINKS; THE CELLS IN A REAL MODULE ARE NOT ALL THE SAME, WHICH IS WHY EVERY ONE IS WATCHED; DETAILS BELOW

FRONT ELEVATION - MODULE WITH ITS TAPS

NOT TO SCALE



NOTES

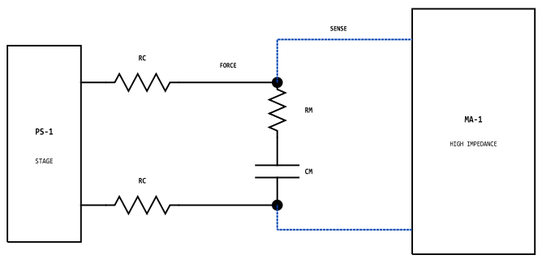
1. REFERENCE ARRANGEMENT OF A BENCH SUPERCAPACITOR MODULE TEST SYSTEM. LETTERS ARE QUANTITIES SET BY DESIGN: NO VOLTAGE, CURRENT, CAPACITANCE, RESISTANCE, TEMPERATURE, COUNT OR TIME VALUE IS GIVEN.
2. THE PLAN SHOWS THE TESTER CABINET TC-1 WITH THE POWER STAGE PS-1 AND THE MEASURING UNIT MA-1, THE CHAMBER CH-1 WITH ITS CABLE PORT PT-1, THE MODULE MU-1, THE FORCE BUSBARS BB-1, THE SENSE WIRES SN-1 AND THE CELL-TAP HARNESS CT-1. THE FRONT ELEVATION SHOWS THE MODULE: FOUR CELLS IN SERIES, THE LINKS, THE TERMINALS AND THE VOLTAGES V1 TO V4 AND VM.
3. DETAIL A: THE FOUR-WIRE CONNECTION. DETAIL B: THE POWER LOOP. DETAIL C: THE PROTECTION CHAIN. THE NUMBER OF CELLS IN A REAL MODULE IS WHATEVER THE MODULE HAS.
4. THE SEQUENCE OF A TEST AND THE CURVES ARE ON SHEET 002. THE POWER MODULES, THE MEASURING INSTRUMENTS AND THE CHAMBER ARE CATALOGUE ITEMS, BOUGHT IN. THE SAFETY GUARDING OF THE BUSBARS IS NOT SHOWN.

ITEMS

ITEM	DESCRIPTION
1	TESTER CABINET TC-1
2	POWER STAGE PS-1
3	MEASURING UNIT MA-1
4	MODULE UNDER TEST MU-1
5	FORCE BUSBARS BB-1
6	SENSE WIRES SN-1
7	CELL-TAP HARNESS CT-1
8	CHAMBER CH-1, PORT PT-1
9	TEMPERATURE SENSOR TS-1

DETAIL A - THE FOUR-WIRE CONNECTION

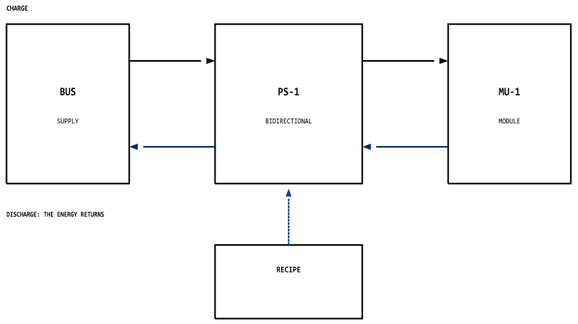
NOT TO SCALE



THE FORCE PAIR CARRIES THE CURRENT AND THE CABLE RESISTANCE RC; THE SENSE PAIR CARRIES NO CURRENT AND SO MEASURES THE MODULE'S OWN RESISTANCE RM AND CAPACITANCE CM AT THE TERMINALS, NOT THE CABLE

DETAIL B - THE POWER LOOP

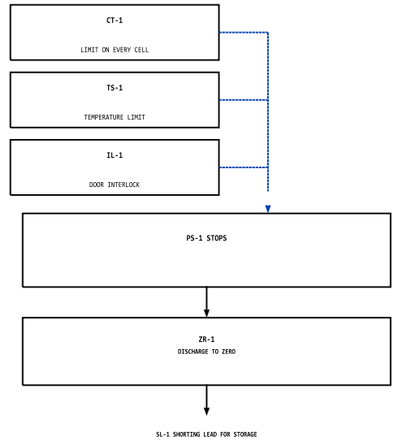
NOT TO SCALE



THE STAGE HOLDS THE CURRENT SET BY THE RECIPE DOWN TO A VERY LOW VOLTAGE; ON DISCHARGE THE ENERGY GOES BACK TO THE SUPPLY, NOT TO A RESISTOR; THE RECIPE STORES THE WINDOW AND THE LIMITS WITH EVERY RESULT

DETAIL C - PROTECTION

NOT TO SCALE



ANY OF THE THREE LIMITS STOPS THE STAGE; THE MODULE IS THEN BROUGHT TO ZERO AND, FOR STORAGE, SHORTED: NOTHING IS LEFT CHARGED

REFERENCE CONFIGURATION - NOT FOR CONSTRUCTION

NEOMETRIX DEFENCE LIMITED

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SUPERCAPACITOR MODULE TEST SYSTEM - REFERENCE CONFIGURATION

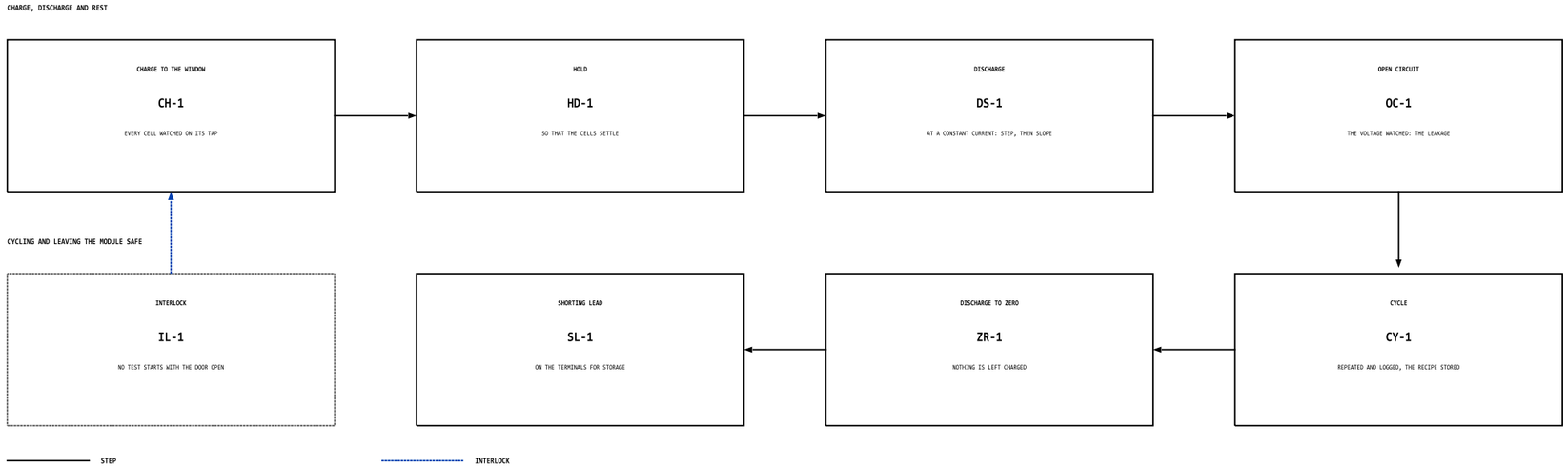
ARRANGEMENT AND DETAILS

THE TEST SYSTEM, THE MODULE AND THREE DETAILS

DWG NO	SCALE @ A3	SHEET	REV
NMX-SCM-117-001	NTS	1 OF 2	A
DATE	UNITS	DRAWN	STATUS
20-11-2026	TAGS ONLY	NMX-DO	REFERENCE

SEQUENCE OF A TEST - SUPERCAPACITOR MODULE TEST SYSTEM

NOT TO SCALE

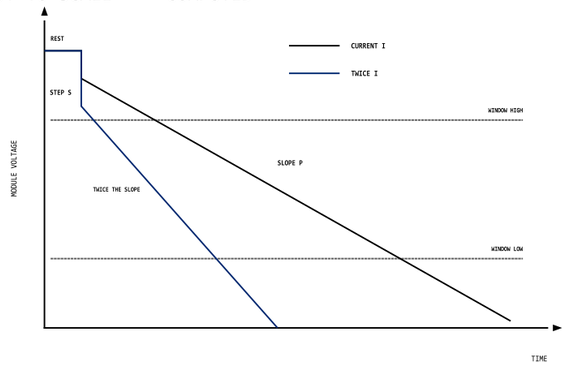


NOTES

1. REFERENCE SEQUENCE AND CURVES OF A BENCH SUPERCAPACITOR MODULE TEST SYSTEM. TAGS AND LETTERS ONLY: NO VOLTAGE, CURRENT, CAPACITANCE, RESISTANCE, TEMPERATURE, COUNT OR TIME VALUE IS GIVEN.
2. THE SEQUENCE: CHARGE CH-1 WITH EVERY CELL WATCHED, HOLD HD-1, DISCHARGE DS-1 AT A CONSTANT CURRENT, OPEN CIRCUIT OC-1 TO WATCH THE LEAKAGE, CYCLE CY-1 WITH THE RECIPE STORED, DISCHARGE TO ZERO ZR-1, AND THE SHORTING LEAD SL-1 FOR STORAGE. THE INTERLOCK IL-1 LETS NO TEST START WITH THE DOOR OPEN.
3. DETAILS A TO C ARE COMPUTED FROM AN IDEAL SERIES R-C MODEL OF A MODULE IN RELATIVE UNITS: A PICTURE OF THE IDEA, NOT A MEASUREMENT. A REAL MODULE'S RESISTANCE AND CAPACITANCE DEPEND ON THE VOLTAGE WINDOW, THE CURRENT AND THE TEMPERATURE. THE ARRANGEMENT IS ON SHEET 001.
4. THE VOLTAGE WINDOW, THE CURRENT AND THE LIMITS OF A REAL TEST COME FROM THE STANDARD OR THE MAKER'S DATASHEET AND ARE SET FOR EACH MODULE.

DETAIL A - THE STEP AND THE SLOPE

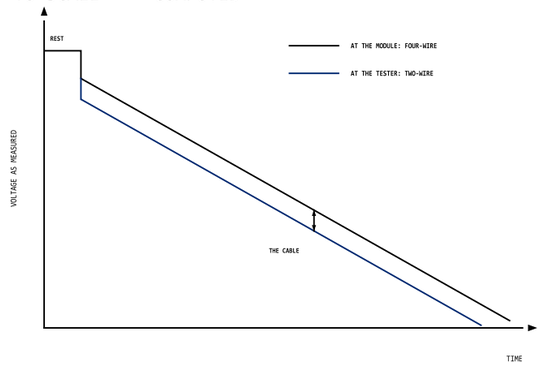
NOT TO SCALE - COMPUTED



AT THE INSTANT THE CURRENT STARTS THE VOLTAGE DROPS BY THE CURRENT TIMES THE RESISTANCE (THE STEP), THEN FALLS IN A STRAIGHT LINE AT THE CURRENT DIVIDED BY THE CAPACITANCE (THE SLOPE); TWICE THE CURRENT GIVES TWICE THE STEP AND TWICE THE SLOPE; COMPUTED IN RELATIVE UNITS: A PICTURE OF THE IDEA, NOT A MEASUREMENT

DETAIL B - THE CABLE IN THE READING

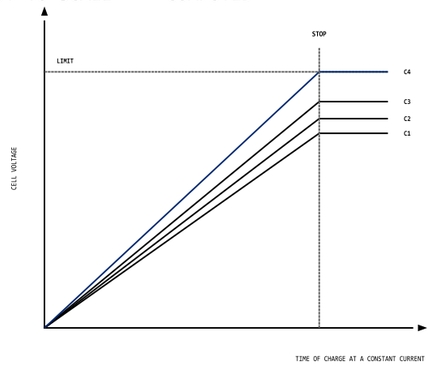
NOT TO SCALE - COMPUTED



THE SAME DISCHARGE SEEN AT TWO PLACES: THE CABLE BETWEEN THE TESTER AND THE MODULE ADDS ITS OWN RESISTANCE, SO THE STEP SEEN AT THE TESTER IS TOO BIG BY THE CABLE'S SHARE, WHILE THE SLOPE IS NOT CHANGED; SENSE WIRES ON THE MODULE TERMINALS LEAVE THE CABLE OUT; COMPUTED IN RELATIVE UNITS: A PICTURE OF THE IDEA, NOT A MEASUREMENT

DETAIL C - THE WEAKEST CELL

NOT TO SCALE - COMPUTED



THE CELLS TAKE THE SAME CHARGE, SO THE ONE WITH THE SMALLEST CAPACITANCE (C4) HAS THE HIGHEST VOLTAGE AND REACHES ITS LIMIT FIRST, WHILE THE MODULE IS STILL BELOW ITS RATING; A TAP ON EVERY CELL SHOWS IT; COMPUTED, RELATIVE UNITS: A PICTURE OF THE IDEA, NOT A MEASUREMENT

REFERENCE CONFIGURATION - NOT FOR CONSTRUCTION

NEOMETRIX DEFENCE LIMITED
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SUPERCAPACITOR MODULE TEST SYSTEM - REFERENCE CONFIGURATION

SEQUENCE AND CURVES

THE SEQUENCE OF A TEST AND THE CURVES OF THE IDEA

DWG NO	SCALE @ A3	SHEET	REV
NMX-SCM-117-002	NTS	2 OF 2	A
DATE	UNITS	DRAWN	STATUS
20-11-2026	TAGS ONLY	NMX-DO	REFERENCE